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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2211

EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,416	MAS ET AL.	
	Examiner	Art Unit	
	William Boddie	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event; however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/27/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Claims 1-8 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-8 of copending Application No. 10/917,846. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

4. Claims 1-8 of this application conflict with claims 1-8 of Application No. 10/917,846. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 5, 6, and 7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 5 states, increasing the biasing voltage when the first signal is **higher** than the second signal. All detailed discussion in the specification and abstract discusses increasing the biasing voltage when the first signal is **lower** than the second signal. Claim 7 is rejected for this same reason, due to the limitation stating, "increasing the biasing voltage when the first signal is higher than the second signal and conversely." Claims 6 and 8 are rejected as claims dependent upon the previously rejected claims 5 and 7.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 3 recite the limitation "the reference node" in the third bullet of claim 1 and line 5 of claim 3. There is insufficient antecedent basis for this limitation in the claim.

6. Claims 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 states, "adapted to increase the biasing voltage when the first signal is **higher** than the second signal and conversely." However, claim 1, of which claim 5 is dependent upon, contradicts this saying, "adapted to increase the biasing voltage when the first signal is **lower** than the second signal and conversely." It appears that the applicant might have intended for claim 5 to mirror the previous limitation stated in claim 1. Claim 6 is once again rejected for being dependent upon a previously rejected claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-3 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. (US 6,518,962) in view of Ishizuka et al. (US 6,756,951).

With respect to claim 1, Kimura discloses, a device for regulating the biasing voltage of column control circuits of an array screen made of LEDs distributed in lines and columns (fig. 1), said device comprising:

first measuring means providing a first signal representative of the voltage of at least one of the columns (16 in fig. 3);

second measuring means providing a second signal representative of the voltage of the reference node (note Iref in fig. 3); and

an adjustment circuit receiving the first and second signals (21a in fig. 3) and being adapted to increase the biasing voltage when the first signal is lower than the second signal and conversely (col. 21 line 57 – col. 22 line 6).

Kimura does not expressly disclose, the column control circuits comprising a current mirror having a reference branch and several duplication branches connected to the biasing voltage, each duplication branch being coupled to a column of the screen, the reference branch being connected to a reference current source providing a desired luminance current.

Ishizuka discloses, second measuring means providing a second signal representative of the voltage of the reference node (note 200 in fig. 8 and CC in fig. 11); the column control circuits comprising a current mirror having a reference branch (CC in fig. 11) and several duplication branches (Q1- Qm in fig. 11) connected to the biasing voltage (Vbe in fig. 11), each duplication branch being coupled to a column of the screen (X1-Xm in fig. 11), the reference branch being connected to a reference current source providing a desired luminance current (Iin in fig. 11).

Kimura and Ishizuka are analogous art because they are directed to a similar problem solving area, namely uniformity among pixel luminance.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include Ishizuka's reference current creation circuitry and column control circuitry in the display device of Kimura. For instance applying the reference created by Ishizuka also being routed to the comparison circuit of Kimura.

The motivation for doing so would have been to compare the actual pixel current with the current that was used to drive the pixel to determine if any loss is taking place in the pixel luminance.

Therefore, it would have been obvious to combine Ishizuka with Kimura for the benefit of compare the LED current with the drive current to obtain the invention as specified in claim 1.

With respect to claim 2, Kimura and Ishizuka disclose, the device of claim 1 (see above).

Ishizuka further discloses, wherein each branch of the current mirror includes a PMOS field effect transistor (Q1-Qm in fig. 11) having a source connected to the biasing voltage, the gates of each branch being connected together, the drain and the gate of the transistor of the reference branch being connected to the reference current source, the drains of the transistors of the duplication branches being connected to the columns (as can be seen in fig. 11 Ishizuka's transistors are oriented in the same way as seen in applicants disclosure on fig. 3).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to construct the column control circuitry as disclosed by Ishizuka and include that circuitry in the display device of Kimura.

The motivation for doing so would have been simplicity of circuitry and the ability to drive each column with an identical amount of current.

Therefore, it would have been obvious to combine Kimura with Ishizuka for the benefit of driving with identical current amounts to obtain the invention as specified in claim 2.

With respect to claim 3, Kimura and Ishizuka disclose, the device of claim 1.

Kimura further discloses, wherein said fist measuring means comprise for each column a diode (110 in fig. 19) having an anode connected to the column (133 in fig. 19) and having a cathode connected to a first observation current source (204 in fig. 19) and to a first input of the adjustment circuit (16' in fig. 19).

Kimura does not expressly disclose, wherein the second measuring means comprise a diode having an anode connected to the reference node and a cathode connected to a second observation current source and to a second input of the adjustment circuit.

Ishizuka discloses, wherein the second measuring means comprise a diode (Qc in fig. 11 is has its base and collector coupled together (col. 6, lines 15-17), thus creating a diode connected transistor. As is obvious to those of ordinary skill in the art a diode connected transistor is equivalent to a diode.) having an anode connected to the reference node and a cathode connected to a second observation current source (Qd

and RQ2 are equivalent to a current source) and to a second input of the adjustment circuit.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to construct the reference current generator of Ishizuka to replace Qc with a diode. Then as shown in Kimura to use that reference current in comparison with the LED drive current.

The motivation for doing so would have been simpler circuitry, and as mentioned above for the ability to compare the two currents of the display device.

Therefore it would have been obvious to combine Kimura and Ishizuka for the benefit of simpler circuitry to obtain the invention as specified in claim 3.

With respect to claim 7, Kimura discloses, a method for regulating the biasing voltage of column control circuits of a screen array made of LEDs distributed in lines and columns comprising the following steps.

providing a first signal representative of the voltage of at least one of the columns; (16 in fig. 3);

providing a second signal representative of the voltage at the reference node; and (note Iref in fig. 3);

and increasing the biasing voltage when the first signal is higher than the second signal and conversely (Kimura discloses altering the biasing voltage based on a comparison between the first signal and the second signal. Kimura also discloses increasing the biasing voltage when the first signal is lower (col. 21 line 57 – col. 22 line

6). It would have been obvious to instead increase the biasing voltage when the first signal is higher).

Kimura does not expressly disclose, the column control circuits comprising a current mirror having a reference branch and several duplication branches connected to the biasing voltage, each duplication branch being coupled to a column of the screen, the reference branch being connected at a reference node to a reference current source providing a desired luminance current, and increasing the biasing voltage when the first signal is higher than the second signal and conversely.

Ishizuka discloses, providing a second signal representative of the voltage at the reference node; and (note 200 in fig. 8 and CC in fig. 11); the column control circuits comprising a current mirror having a reference branch (CC in fig. 11) and several duplication branches (Q1- Qm in fig. 11) connected to the biasing voltage (Vbe in fig. 11), each duplication branch being coupled to a column of the screen (X1-Xm in fig. 11), the reference branch being connected at a reference node to a reference current source providing a desired luminance current (Iin in fig. 11).

At the time of the invention it would have been obvious to one of ordinary skill in the art to include Ishizuka's reference current creation circuitry and column control circuitry in the display device of Kimura. For instance applying the reference created by Ishizuka also being routed to the comparison circuit of Kimura. Then increasing the biasing current when the first signal is larger than the second signal.

The motivation for doing so would have been to compare the actual pixel current with the current that was used to drive the pixel and to drive an even brighter display if the first signal is larger than the second signal.

Therefore, it would have been obvious to combine Ishizuka with Kimura for the benefit of a brighter display to obtain the invention as specified in claim 7.

With respect to claim 8, Kimura and Ishizuka disclose, the device of claim 7 (see above).

Neither Kimura nor Ishizuka explicitly disclose, wherein the fist signal is an image of the maximum voltage of the activated LEDs.

It is within the scope of normal display device operation to at times supply an activated LED with the maximum voltage possible for that pixel.

As such at the time of the invention it would have been obvious to a person of ordinary skill in the art to drive an activated LED with a maximum voltage possible, as such this maximum voltage would have then been compared in the display device disclosed by Kimura and Ishizuka.

The motivation for doing so would have been to achieve the brightest display possible.

Therefore, it would have been obvious to combine Kimura with Ishizuka for the benefit of a bright display to obtain the invention as specified in claim 8.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. (US 6,518,962) in view of Ishizuka et al. (US 6,756,951) and further in view of Bu (US 6,433,488).

With respect to claim 4, Kimura and Ishizuka disclose, the device of claim 3 (see above).

Kimura further discloses, wherein the cathodes of all the diodes are connected to the first input of the adjustment circuit by a switch (303 in fig. 18).

Neither Kimura nor Ishizuka expressly disclose, a capacitor being connected between the first input of the adjustment circuit and affixed voltage node.

Bu discloses, a capacitor (23 in fig. 2) being connected between the first input of the adjustment circuit (current comparator in fig. 2) and affixed voltage node (note that 23 is grounded in fig. 2).

Bu, Kimura, and Ishizuka are analogous art because they are from the same field of endeavor namely, current drivers for display devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a switch and capacitor in the combined device of Kimura and Ishizuka.

The motivation for doing so would have been to allow the current to be measured sequentially in each column line (Kimura, col. 35, lines 46-50).

Therefore it would have been obvious to combine Bu, Kimura, and Ishizuka for the benefit of measuring the current lines sequentially to obtain the invention as specified in claim 4.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sabouri (US 6,774,723) discusses the equivalence of a diode-

connected transistor and a diode (col. 4, lines 50-60). Kimura (US 6,710,548) discloses another driving current correction circuit.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 8:00 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wlb
9-28-05

REGINA LIANG
PRIMARY EXAMINER